Practitioner's Docket No.: 989_001DIV1 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

James E. Moon et al.

Ser. No.: Not Assigned

Filed: Concurrently Herewith

Parent Appln. Information:

Serial No. 09/334,408

Filed: June 16, 1999

For: METHOD FOR FABRICATING MEMS AND MICROFLUIDIC DEVICES USING LATENT MASKING TECHNIQUE

Box Divisional Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

"EXPRESS MAIL" mailing label number EL73097773US.

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 addressed to the **Box Divisional Patent Application, Assistant Commissioner for Patents, Washington D.C. 20231** on November 2, 2001.

Cheryl M. Nichols

Cheryl M. Nichols

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows before examination thereof:

In the Claims:

Please cancel claims 4-23.

Please amend claims 1-3 as follows:

1. (Amended) A method for fabricating a microelectromechanical device, comprising the steps of:

a) providing a silicon substrate having first and second opposing surfaces;

b) forming first and second silicon oxide layers on said first and second surfaces of said substrate, respectively;

c) coating a first photoresist layer on said first silicon oxide layer;

d) defining a first pattern on said first photoresist layer;

e) transferring said first pattern onto said first silicon oxide layer using dry etching;

f) performing, without coating a protective layer onto said first pattern, at least one additional processing step that does not perturb said transferred first pattern while said silicon substrate under said first pattern is protected by said first silicon

oxide layer; and

g) dry etching, after the step of performing said at least one additional processing step, said first pattern into said silicon substrate such that the planar dimensions of said first pattern are reproduced in said silicon substrate.

2. (Amended) The method of claim 1, wherein said at least one additional processing step comprises coating, defining, and transferring at least one additional pattern onto at least one of said first and second silicon oxide layers using dry etching.

3. (Amended) The method of claim 2, wherein said at least one additional processing step further comprises dry etching said at least one additional pattern into said silicon substrate.

REMARKS

Claims 1-3 are pending herein. Claims 1-3 are amended, and claims 4-23 are cancelled.

The following is provided to assist the Examiner in his examination of the claims. Three etching techniques are used to create microelectromechanical (MEMS) and/or microfluidic devices. These techniques can be used singly or in various combinations with each other. These techniques are referred to in the description as Latent Masking, SMILE, and delayed LOCOS.

Latent Masking defines a mask in a persistent material like silicon oxide that is held abeyant after definition while intervening processing operations are performed. The intervening steps do not disturb nor are disturbed by the mask. After the intervening steps are performed, the latent oxide pattern is then used to mask an etch. Latent Masking is presented in claims 1-3, and is the subject of the claims of this divisional application.

SMILE, which is an acronym based on "simultaneous multi-level etching", provides a process sequence wherein a first pattern may be given an advanced start relative to a second pattern in etching into an underlying material, such that the first pattern may be etched deeper, shallower, or to the same depth as the second pattern. This process allows etching two different patterns into a substrate such that the final depth of the two patterns is independently controlled. SMILE is presented in claim

4. A variant of SMILE is presented in claim 5 in which the SMILE technique is applied to three patterns instead of only two patterns. These claims are cancelled in this application.

Delayed LOCOS provides a means of defining a contact hole pattern at an early stage of a process, then using the defined pattern at a later stage to open the contact holes. This is an alternative to the well known process of LOCOS (local oxidation of silicon) which permits the initial patterning to be done when there is no surface topography to interfere with the uniform and continuous coating of the photoresist, unlike the LOCOS process which is done immediately prior to metallization. Delayed LOCOS is presented in claim 6. This claim is cancelled in this application.

A combination of all three techniques is used in fabricating an LC/ESI device, as presented in claims 10-12. The combination of all three techniques, i.e., SMILE, Latent Masking, and Delayed LOCOS, but not specifically applied to making an LC/ESI device, is presented in claims 7-9. These claims are cancelled in this application.

A combination of SMILE and Delayed Locos is used in fabricating an ESI device, as presented in claims 14-16. A combination of SMILE and Delayed Locos, but not specifically applied to making an ESI device, is presented in claim 13. These claims are cancelled in this application.

A combination of Latent Masking and Delayed LOCOS is used in fabricating an LC device, as presented in claims 20-22. A combination of Latent Masking and Delayed LOCOS, but not specifically applied to making an LC device, is presented in claims 17-19. These claims are cancelled in this application.

A combination of SMILE and Latent Masking is presented in claim 23. This claim is cancelled in this application.

Thus, the independent claims cover three techniques and combinations thereof, as well as three devices made with three of the combinations of techniques. Perhaps it would be useful to recapitulate the claims and their techniques in claim sequence.

Claims 1-3: Latent Masking

Claim 4: SMILE (2 patterns)

Claim 5: SMILE (3 patterns)

Claim 6: Delayed LOCOS

Claims 7-9: SMILE plus Latent Masking plus Delayed LOCOS

Claims 10-12: SMILE plus Latent Masking plus Delayed LOCOS as applied to making an integrated LC/ESI device

Claim 13: SMILE plus Delayed LOCOS

Claims 14-16: SMILE plus Delayed LOCOS as applied to making an ESI device

Claims 17-19: Latent Masking plus Delayed LOCOS

Claims 20-22: Latent Masking plus Delayed LOCOS as applied to making an LC device

Claim 23: SMILE plus Latent Masking

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

If the Examiner believes that contact with Applicant's attorney would be advantageous toward the disposition of this case, the Examiner is herein requested to call Applicant's attorney at the telephone number noted below.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0289.

Respectfully submitted,

WALL MARJAMA & BILINSKI, LLP

Dated: 11/2/01

By: _____
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PATENT TRADEMARK OFFICE

"VERSION WITH MARKINGS TO SHOW CHANGES MADE."

In the Claims:

1. (Amended) A method for fabricating a microelectromechanical device, comprising the steps of:

a) providing a silicon substrate having first and second opposing surfaces;

b) forming first and second silicon oxide layers on said first and second surfaces of said substrate, respectively;

c) coating a first photoresist layer on said first silicon oxide layer;

d) defining a first pattern on said first photoresist layer;

e) transferring said first pattern onto said first silicon oxide layer using dry etching;

f) performing, without coating a protective layer onto said first pattern, at least one additional processing step that does not perturb said transferred first pattern while said silicon substrate under said first pattern is protected by said first silicon oxide layer; and

g) dry etching, after the step of performing said at least one additional processing step, said first pattern into said silicon substrate such that the planar dimensions of said first pattern are reproduced in said silicon substrate.

2. (Amended) The method of claim 1, wherein said at least one additional processing step comprises coating, defining, and transferring at least one additional pattern onto at least one of said first and second silicon oxide layers using dry etching.

3. (Amended) The method of claim 2, wherein said at least one additional processing step further comprises dry etching said at least one additional pattern into said silicon substrate.